Case Docket No. PHA 23,843

THE COMMISSIONER OF PATENTS AND TRADEMARKS, Washington, D.C. 20231

Enclosed for filing is the patent application of Inventor:
NAVEED MAJID, TON MOBERS and SATYEN MUKHERJEE

MULTIPLE SEMICONDUCTOR CHIP (MULTI-CHIP) MODULE FOR USE IN HIGH-POWER APPLICATIONS

ENCLOSED ARE:

[X] Appointment of Associates;
[X] Information Disclosure Statement, Form PTO-1449 and copies of documents listed therein;
[ ] Preliminary Amendment;
[X] Specification (10 Pages of Specification, Claims, & Abstract);
[X] Declaration and Power of Attorney:
(4 Pages of a [X]fully executed [ ]unsigned Declaration);
[X] Drawing (1 sheet of [X]informal [ ]formal sheets);
[ ] Certified copy of application Serial ;
[X] Authorization Pursuant to 37 CFR §1.136(a)(3)
[ ] Other: ;
[X] Assignment to PHILIPS ELECTRONICS NORTH AMERICA CORPORATION.

FEE COMPUTATION

CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE - $760.00
Total Claims	8 - 20 =		X $18 =	0.00
Independent Claims	2 - 3 =		X $78 =	0.00
Multiple Dependent Claims, if any			$260 =	0.00
TOTAL FILING FEE			=	$760.00

Please charge Deposit Account No. 14-1270 in the amount of the total filing fee indicated above, plus any deficiencies. The Commissioner is also hereby authorized to charge any other fees which may be required, except the issue fee, or credit any overpayment to Account No. 14-1270.

[ ]Amend the specification by inserting before the first line as a centered heading --Cross Reference to Related Applications--; and insert below that as a new paragraph --This is a continuation-in-part of application Serial No. , filed , which is herein incorporated by reference--.

CERTIFICATE OF EXPRESS MAILING

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I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

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Typed Name

Signature

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MULTIPLE SEMICONDUCTOR CHIP (MULTI-CHIP) MODULE FOR USE IN HIGH-POWER APPLICATIONS

BACKGROUND OF THE INVENTION

The invention is in the field of semiconductor devices, and relates more specifically to multiple semiconductor chip (hereinafter multi-chip) modules for use high-power applications.

Multi-chip module technology has recently been applied to integrated circuits used in high power applications, such as power supplies and electronic ballast circuits. Such multi-chip modules typically include at least a power semiconductor chip and a control semiconductor chip mounted on an electrically conductive (typically metal) heat sink. In the prior art, one or more of the chips employed in the module must be electrically insulated from the metal heat sink in order to maintain electrical isolation, thus requiring a relatively complicated structure which is costly to manufacture. Additionally, such a configuration is not ideal in terms of electrical performance, because electrically isolating one or more chips from the metal heat sink and having the heat sink float at other than ground potential may result in electromagnetic interference (EMI).

A typical prior-art device configuration is shown in Japanese patent abstract JP 6-169057A. In the elementary multi-chip module shown in this reference, one chip is shown as soldered directly to a heat sink, while a second chip is provided on an electrode plate, which is in turn provided on an insulating ceramic plate provided

on the heat sink.

While the foregoing structure permits the fabrication of a multi-chip module incorporating different chip types and functions, it is relatively complicated and therefore uneconomical to manufacture, and in certain applications structures of this type will generate electromagnetic (EMI) radiation.

Accordingly, it would be desirable to have a multi-chip module for use in high-power applications which is simple in construction and therefore economical to fabricate, and in which performance parameters such as reduced EMI are enhanced.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a multi-chip module for use in high-power applications which is simple in construction, economical to fabricate, and capable of offering enhanced performance.

In accordance with the invention, these objects are achieved in a multi-chip module of the type described above in which a plurality of semiconductor chips are all directly mounted on an electrically conductive heat sink without the use of a separate electrical insulation layer.

In a preferred embodiment of the invention, the multi-chip module includes at least a power semiconductor chip having a silicon-on-insulator (SOI) device and a control semiconductor chip having a semiconductor device with a substrate connected to ground potential, with both the power semiconductor chip and the control

semiconductor chip being directly mounted on the electrically conductive heat sink without the use of a separate electrical insulation layer.

In further preferred embodiments of the invention, the control semiconductor chip includes BIMOS, bipolar, or CMOS devices and has a substrate connected to ground potential.

Multi-chip modules in accordance with the present invention offer a significant improvement in that a simple, economical configuration having improved performance characteristics is achieved.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

BRIEF DESCRIPTION OF THE DRAWING

The invention may be more completely understood with reference to the following description, to be read in conjunction with the accompanying drawing, in which the single Figure shows a simplified cross-sectional view of a multi-chip module in accordance with a preferred embodiment of the invention.

It should be understood that the single Figure of the drawing is not drawn to scale.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the simplified cross-sectional view of the single Figure, a multiple semiconductor chip (multi-chip) module 10 for use in high-

power circuit applications is shown. The multi-chip module 10 includes an electrically conductive heat sink 20, typically a metal heat sink of copper or aluminum, on which are directly mounted a plurality of semiconductor chips, such as chips 30 and 40 shown in simplified form within bold rectangles in the Figure. It should be noted that the semiconductor chips 30 and 40 are directly mounted on the conductive heat sink 20 without the use of a separate electrical insulation layer as is typically required in the prior art.

In the example shown, semiconductor chip 30 is a power semiconductor chip, here shown as a Silicon-On-Insulator (SOI) device having a semiconductor substrate 38, a buried insulating layer 39, and an SOI layer 32 having at least one semiconductor device symbolically shown by region 34 provided therein. Electrical connections to the semiconductor device 34 are symbolically shown by the single electrode 36, although it will be apparent that in an actual device more than one connection will typically be provided. By placing all of the high-voltage and high-power components of the multi-chip module on SOI power semiconductor chip 30, it becomes possible to directly mount the semiconductor chip on the conductive heat sink 20 without the use of a separate electrical insulation layer, since the portions of the chip connected to high voltage are insulated from the substrate 38 by oxide insulation layer 36 within the chip itself. Power semiconductor chip 30 can be directly mounted on the conductive heat sink 20 by known conventional methods, such as soldering or

gluing with a conductive glue. If power semiconductor chips other than SOI chips are used, they must be capable of operating with their substrates connected directly to the conductive heat sink.

The multi-chip module 10 also includes a control semiconductor chip 40 shown in simplified form in the Figure, also directly mounted on the conductive heat sink 20 without the use of a separate electrical insulation layer. The control semiconductor chip 40 is symbolically shown by a substrate 46 in which is formed at least one semiconductor device 42, with electrical connections to the device being symbolically shown by the single connection electrode 44.

In order to further reduce the manufacturing cost of multi-chip module 10, the control semiconductor chip 40 can employ a low-cost technology such as BIMOS, bipolar, or CMOS to implement the control circuit devices symbolically shown by reference numeral 42. It will be recognized that various technologies may be used to fabricate the control circuitry, the only limitation being that the back of the chip (substrate 46) must be capable of being directly mounted on the conductive heat sink 20, which will typically be at ground potential. A further advantage of having the conductive heat sink 20 and the substrate of the control semiconductor chip 40 at ground potential is that electromagnetic radiation (EMI) will be reduced, since the grounded heat sink cannot serve as an antenna to radiate interference signals. As in the case of power semiconductor chip 30, control semiconductor chip 40 may be mounted to the conductive heat sink 20 by soldering or other conventional

electrically conductive fastening technique.

It will be understood that while the simplified representative structure shown in the single Figure depicts a preferred embodiment of the invention, numerous variations in device geometry, configuration and number of chips used are contemplated within the scope of the invention. Nevertheless, it is noted that several advantages accrue by using a configuration in accordance with the preferred embodiment. By directly mounting all of the semiconductor chips on the conductive heat sink without the use of a separate electrical insulation layer, the fabrication process is simplified and made more economical, EMI is reduced and efficient heat transfer is ensured. Additionally, by using a low-cost technology such as BIMOS, CMOS or bipolar for the control semiconductor chip(s), further advantages in economy and performance are obtained. Finally, by using an SOI device as the power semiconductor chip, direct mounting of this chip is facilitated while permitting great flexibility in high-voltage device design even though the substrate is typically grounded, since the active portion of the device is internally insulated from the substrate.

In the foregoing manner, the present invention provides a multi-chip module for use in high-power applications which is simple in structure, economical to fabricate and which offers performance advantages.

While the invention has been particularly shown and described with reference to several preferred embodiments thereof, it will be

understood by those skilled in the art that various changes in form and detail may be made without departing from the spirit or scope of the invention. In this application it should be understood that the word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements, and that the word "comprising" does not exclude the presence of other elements or steps than those described or claimed.

What is claimed is:

1. A multiple semiconductor chip (multi-chip) module for use in high-power applications, comprising at least a power semiconductor chip and a control semiconductor chip mounted on an electrically conductive heat sink, wherein said power semiconductor chip comprises a Silicon-On-Insulator (SOI) device and said control semiconductor chip comprises a semiconductor device having a substrate connected to ground potential, and said power semiconductor chip and said control semiconductor chip are directly mounted on said electrically conductive heat sink without the use of a separate electrical insulation layer.

2. A multi-chip module as in claim 1, wherein said control semiconductor chip semiconductor device comprises a BIMOS device.

3. A multi-chip module as in claim 1, wherein said control semiconductor chip semiconductor device comprises a CMOS device.

4. A multi-chip module as in claim 1, wherein said control semiconductor chip semiconductor device comprises a bipolar device.

5. A multi-chip module as in claim 1, wherein said conductive heat sink is connected to ground potential.

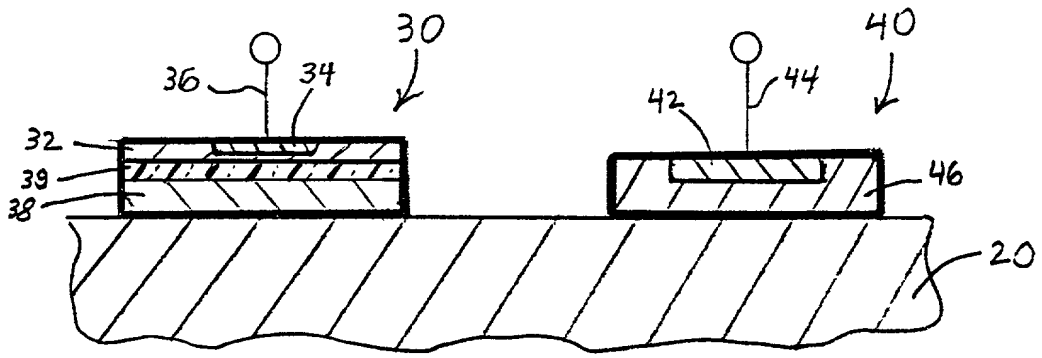
6. A multi-chip module as in claim 1, wherein said conductive heat sink comprises a metal.

7. A multi-chip module a in claim 6, wherein said metal comprises copper.

8. A multiple semiconductor chip (multi-chip) module for use in high-power applications, comprising a plurality of semiconductor chips all directly mounted on an electrically conductive heat sink without the use of a separate electrical insulation layer.

ABSTRACT OF THE DISCLOSURE

A multiple semiconductor chip (multi-chip) module for use in high-power applications includes at least a power semiconductor chip and a control semiconductor chip mounted on an electrically conductive heat sink. The power semiconductor chip may be a Silicon-On-Insulator (SOI) device and the control semiconductor chip may be a semiconductor device having a substrate connected to ground potential. The power semiconductor chip and the control semiconductor chip are directly mounted on the electrically conductive heat sink without the use of a separate electrical insulation layer in order to obtain a multi-chip module which is simple and economical to manufacture, and which offers superior performance characteristics.



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

NAVEED MAJID ET AL

Atty. Docket

PHA 23,843

Serial No.

Filed: CONCURRENTLY

MULTIPLE SEMICONDUCTOR CHIP (MULTI-CHIP) MODULE FOR USE IN HIGH-POWER APPLICATIONS

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:
Steven R. Biren (Registration No. 26,531)
c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, 580 White Plains Road, Tarrytown, New York 10591, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,

Jack E. Haken, Reg. 26,902
Attorney of Record

Dated at Tarrytown, New York
this 15TH day of November 1999.

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DECLARATION and POWER OF ATTORNEY

700845

Attorney's Docket No. PHA 23,843

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled MULTIPLE SEMICONDUCTOR CHIP (MULTI-CHIP) MODULE FOR USE IN HIGH-POWER APPLICATIONS

The specification of which (check one)

XX is attached hereto.

___ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by the amendment(s) referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulation, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (DAY, MONTH, YEAR)	PRIORITY CLAIMED UNDER 35 U.S.C. 119

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application (s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PRIOR UNITED STATES APPLICATION(S)

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Algy Tamoshunas, Reg. No. 27,677

Jack E. Haken, Reg. No. 26,902

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO:
Corporate Patent Counsel; U.S. Philips Corporation; 580 White Plains Road; Tarrytown, NY 10591	(name and telephone No.) Steven R. Biren (914) 333-9630

Dated: 10/29/99		INVENTOR'S SIGNATURE:		
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Full Name of Inventor	Last Name	FIRST NAME	Middle Name	
Residence & Citizenship	City	STATE OR FOREIGN COUNTRY	Country of Citizenship	
Post Office Address	Street	CITY	State or Country	Zip Code

DECLARATION and POWER OF ATTORNEY

700845

Attorney's Docket No.
PHA 23,843

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled MULTIPLE SEMICONDUCTOR CHIP (MULTI-CHIP) MODULE FOR USE IN HIGH-POWER APPLICATIONS

The specification of which (check one)

XX is attached hereto.

___ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

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